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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,805	01/13/2004	Takafumi Noda	9319S-000608	1517

27572 7590 11/16/2005

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/756,805	NODA, TAKAFUMI	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *3-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/04,9/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to applicant's election filed August 26, 2005.

Election/Restrictions

Claims 3-5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on August 26, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 6 rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki (JP08-078674).

Kawasaki (Fig. 1) discloses:

(cl. 1, 6) a semiconductor device comprising: a gate insulating film (3) provided on a semiconductor layer (1), a gate electrode (4) provided on the gate insulating film, and a source region and a drain region (6a, b) provided in the semiconductor layer at two sides of the gate electrode, wherein the source and the drain regions comprise first impurity diffusion layers (e.g. source & drain) formed of a specific impurity introduced in the semiconductor layer adjacent two sides of the gate electrode, and second impurity diffusion layers (7a,b) provided in the semiconductor layer adjacent the first

impurity diffusion layers and opposite from the gate electrode, the second impurity diffusion layers being in contact/abutting with the first impurity diffusion layers, and wherein the first impurity diffusion layers comprise a diffusion suppression impurity for suppressing diffusion of the specific impurity into the semiconductor layer (Abstract); (cl. 2) wherein the diffusion suppression impurity is located in the semiconductor layer under (e.g. in a region below) the gate electrode.

Claims 1, 2 and 6 rejected under 35 U.S.C. 102(b) as being anticipated by Fujitsu (JP10-256839).

Fujitsu[1] (Fig. 1a-d) discloses:

(cl. 1, 6) a semiconductor device comprising: a gate insulating film (4) provided on a semiconductor layer (1), a gate electrode (5) provided on the gate insulating film, and a source region and a drain region (6s, d) provided in the semiconductor layer at two sides of the gate electrode, wherein the source and the drain regions comprise first impurity diffusion layers (e.g. source & drain) formed of a specific impurity introduced in the semiconductor layer adjacent two sides of the gate electrode, and second impurity diffusion layers (3) provided in the semiconductor layer adjacent the first impurity diffusion layers and opposite from the gate electrode, the second impurity diffusion layers being in contact/abutting with the first impurity diffusion layers, and

[1] Likewise the cited pertinent art could have used to anticipate applicant's claim.

wherein the first impurity diffusion layers comprise a diffusion suppression impurity for suppressing diffusion of the specific impurity into the semiconductor layer (e.g. s/d are p type; same as applicant SPEC Par. 0040);

(cl. 2) wherein the diffusion suppression impurity is located in the semiconductor layer under (e.g. in a region below) the gate electrode.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. He prior art discloses in: Madhukar (U.S 2002/0135023) and Chatterjee (U.S. 2003/0102512) the use of a first impurity on sides of a gate with a second impurity in contact with first impurity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
November 9, 2005

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800